REMARKS

Claims 28-41 have been canceled. Claims 21 and 27 have been amended. New claims 42-52 have been added. Proposed drawing revisions for Figs. 29-33 are submitted herewith to satisfy a requirement of the Examiner. Examination of the amended application is respectfully requested.

The Examiner requires that Figs. 29-33 be labeled "Prior Art." The required copies of these figures, marked in red with the change, are submitted herewith.

The Examiner also objected to the drawings on the grounds that the "ball-type electrodes" claimed in claims 27, 34 and 41, are not illustrated. Claim 27 has been amended, to characterize the electrodes as "solder balls". Claims 34 and 41 have been canceled. Moreover, Figs. 21 and 24 illustrate electrodes on a wafer (or portion thereof) clearly shown as ball-type, and properly identified as "ball type electrodes" or "solder balls" (see second paragraphs on page 27 and page 28) which relate to the embodiment of Figs. 21 and 24. Therefore, the objection is moot as to claims 34 and 41 and is traversed as to claim 27. The objection accordingly should be withdrawn.

The Examiner objected to claim 28. However, claim 28 has been canceled.

The Examiner rejected claims 21-41 under 35 USC 112, second paragraph, as being indefinite. The rejection as to claims 28-41 is moot since these claims have been canceled. The rejection as to claim 27 relates to the drawing objection relating to "ball type" as discussed above. The rejection is

traversed and should be withdrawn for the same reasons given for the traversal of the objection to the drawing with respect to claim 27. The rejection accordingly should be withdrawn as to claim 27.

As to claims 21-22, the Examiner states that the text "dividing the wafer into a plurality of semiconductor devices" is unclear. However, the applicant does not understand the confusion. When the wafer is divided, then according to both the claim and the specification, a plurality of semiconductor devices are produced. This is fully consistent with the text of the specification on pages 24 and 27 quoted by the Examiner. "The wafer to be measured 401 is resin coated and is ultimately divided into a plurality of CSP devices 411." Whether the ultimate devices are resin coated or completely resin coated is no consequence. For these reasons the present claims are deemed to be in full compliance with the requirements of 35 USC 112, second paragraph, and the rejection accordingly should be withdrawn.

The Examiner also rejected claims 21-41 under 35 USC 102(e) as being anticipated by *Nakata et al.* Claim 21 has been amended and claims 28-41 have been canceled. It is submitted that the rejection is inapplicable to the pending claims 21-27.

Differences between the invention as claimed in the amended independent claim 21 and the new independent claim 44 of the application, and the cited reference (*Nakata et al.* USP 6,297,658 B1) are outlined below.

A feature of the invention is that electrical functions of the circuit elements are tested while the semiconductor wafer is exposed to convective air within the burn-in apparatus. In one embodiment, this constitutes testing the electrical functions of the circuit element while the surface of the semiconductor wafer at which the plurality of electrodes are not formed is exposed to convective air within the burn-in apparatus. Thus, claim 21 has been amended to state, and the new claim 44 of the application states, respectively as a step of the testing method, "testing the circuit elements in the burn-in apparatus for electrical functions, through the electrodes, with the wafer exposed to convective air in the burn-in apparatus" and "testing the circuit elements in the burn-in apparatus for electrical function, through electrodes, with the second surface of the semiconductor wafer exposed to a convective layer in the burn-in apparatus".

This feature is described with reference to the seventh embodiment of the invention described at pages 23-26, particularly at page 23 of the specification and Fig. 13 of the drawings. In this embodiment, a semiconductor device test apparatus e7 assumes a structure that includes a circuit board 303, a film 305, a positioning plate 307 and a holding plate 309. The specification goes on to state in part:

> ***A plurality of ventilating through holes 309b are formed at the holding plate 309. This makes it possible to expose the wafer to be measured 401 to the air that circulates through convection when, for instance, a burn-in is implemented on the wafer to be measured 401. . . .***

The only holes though which a gas is intended to pass during the process disclosed *Nakata et al.* (USP 6,297,658 B1), are not in a holding element or corresponding element and not for any purpose related to passing atmospheric air to a wafer during a burn-in. That is, *Nakata et al.* merely teach that the electrode pad 16 at the semiconductor wafer 10 and the bump 17 are electrically connected with each other by inserting the semiconductor wafer 10 into the wafer burn-in cassette and eliminating (with connection holes 26 in the probe card 12 the difference between the pressures at the first sealed space 15 and the second sealed space 25 which are separated from each other by the probe card 12 (see column 6, line 64 ~ column 7, line 21). Thus, in the wafer burn-in cassette of *Nakata et al.*, the purpose of the connection holes is to permit a burn-in test on a wafer to be conducted in a state in which the pressure difference between the first sealed space 15 and the second sealed space 25 is eliminated. This has nothing at all to do with testing circuit elements in a burn-in apparatus, "with the wafer exposed to convective air in the burn-in apparatus" as stated in claim 21 (or over a surface of the semiconductor wafer at which no electrodes are formed as stated in new claim 44); as by holes in a holding plate. In other words, *Nakata et al.* does not disclose or suggest in any way whatsoever that a burn-in test is conducted while the atmospheric air moves through convection across a wafer. The holes in the probe card 12 between the first sealed space 15 and the second sealed space 25 are for the purpose of equalizing pressure and not to not provide or suggest providing atmospheric air moving through convection over a semiconductor wafer.

For this reason, it is believed clear that the invention recited in the amended independent claim 21 and the new independent claim 44 adopt a structure which is completely different from the structure disclosed in the invention of *Nakata et al.* Moreover, the dependent claims recite other patentably distinguishing features of the invention. Therefore, based on the above, it is submitted that the application is in condition for allowance, and such a Notice with allowed claims 21-27 and 42-52, is earnestly solicited.

Respectfully submitted,

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Date

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MARKED-UP CLAIMS

--21. (Amended) A method for manufacturing semiconductor devices, the method comprising:

providing a semiconductor wafer with a wafer surface having a plurality of circuit elements formed thereon;

forming on the wafer surface a plurality of electrodes connected to the circuit elements;

inserting the wafer into a burn-in apparatus;

testing the circuit elements in the burn-in apparatus for electrical functions, through the electrodes, with the wafer exposed to convective air in the burn-in apparatus; and

dividing the wafer into a plurality of semiconductor devices.

27. A method according to claim 21, [wherein the plurality of electrodes are ball-type] further comprising the step of forming a plurality of solder balls as the electrodes.

FIG. 29

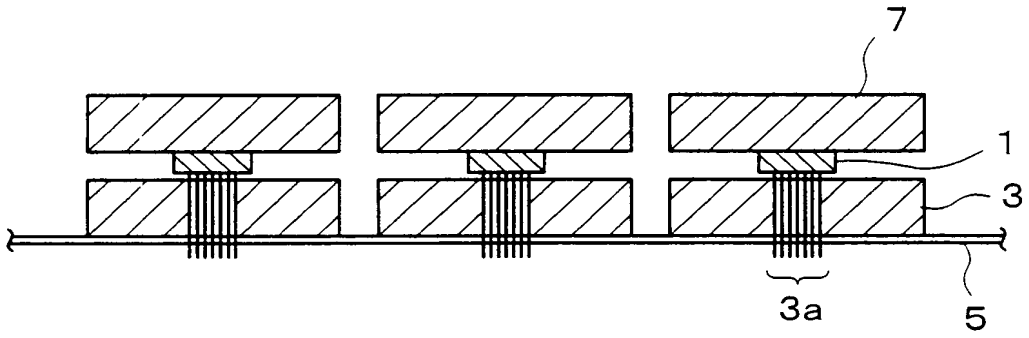

FIG. 30

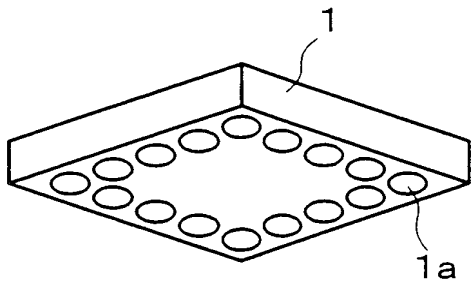

FIG. 31

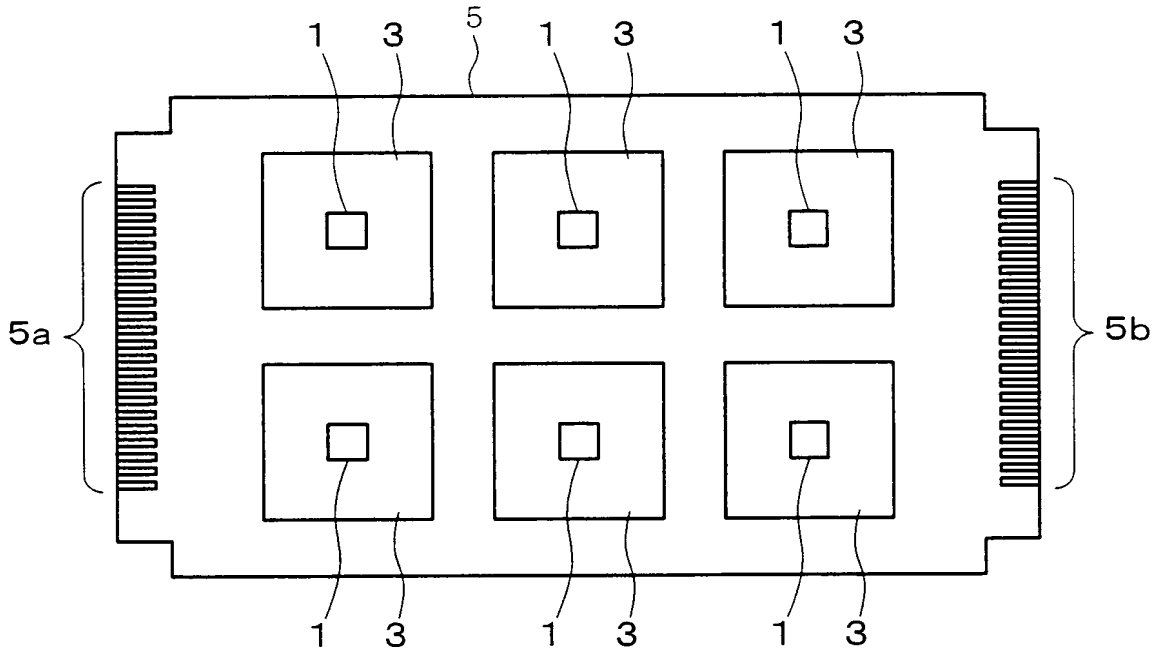

FIG. 32

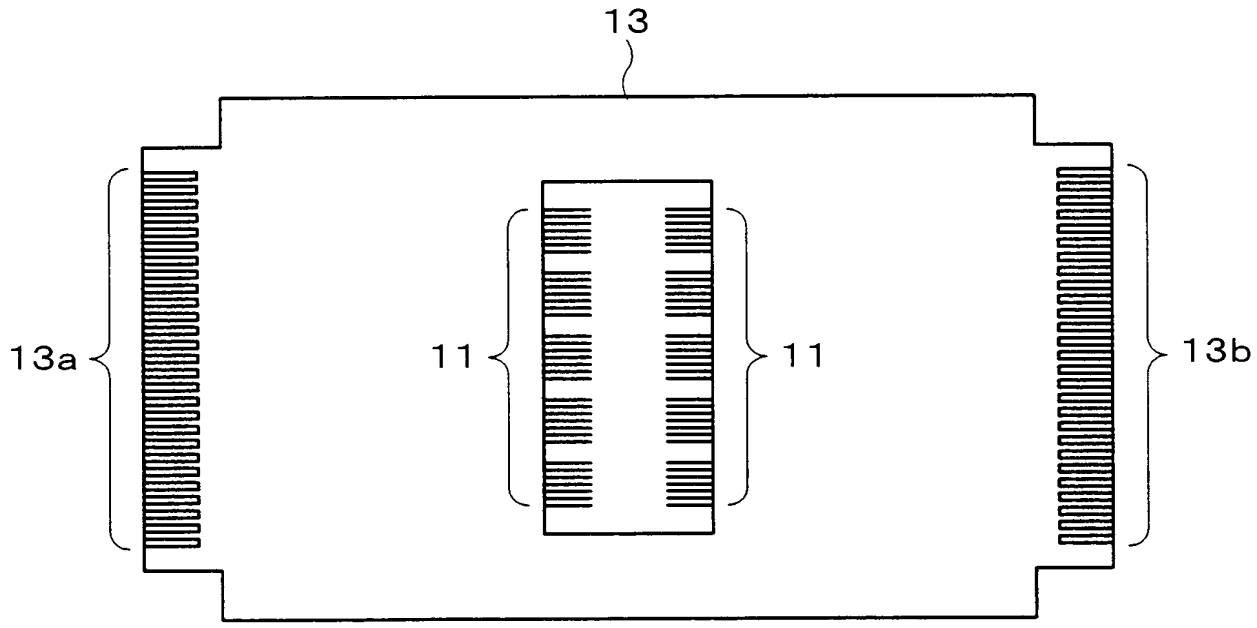

FIG. 33